IN THE SPECIFICATION

Please replace the following paragraphs:

Please replace paragraph **[0008]** with the following amended paragraph:

[0008] FIG. 1 is a block diagram of an embodiment of the disclosed information handling system.

Please replace paragraph **[0012]** with the following amended paragraph:

[0012] IHS 100 includes a power supply 105 with self-diagnosis capabilities. Power supply 105 is coupled via connector 110 to system board 115 to provide power to components on system board 115. System board 115 includes a processor 120 such as an Intel Pentium series processor or one of many other processors currently available. An Intel Hub Architecture (IHA) chipset 125 provides IHS 100 with glue-logic that connects processor 120 to other components of IHS 100. Chipset 125 carries out graphics/memory controller hub functions and I/O functions. More specifically, chipset 125 acts as a host controller which communicates with a graphics controller 130 coupled thereto. Graphics controller 130 is coupled to a display 135. Chipset 125 also acts as a controller for main memory 140 which is coupled thereto. Chipset 125 further acts as an I/O controller hub (ICH) which performs I/O functions. Input devices 145 such as a mouse, keyboard, and tablet, are also coupled to chipset 125 at the option of the user. A universal serial bus (USB) 140 or other I/O bus is coupled to chipset 125 to facilitate the connection of peripheral devices to IHS 100. ~~System~~ The system basic input-output system (BIOS) 150 is coupled to chipset 125 as shown. BIOS 150 is stored in nonvolatile memory such as CMOS or FLASH memory. A network interface controller (NIC) 155 is coupled to chipset 125 to facilitate connection of system 100

to other information handling systems. A media drive controller 160 is coupled to chipset 125 so that devices such as media drive 165 can be connected to chipset 125 and processor 120. Devices that can be coupled to media drive controller 160 include CD-ROM drives, DVD drives, hard disk drives and other fixed or removable media drives. IHS 100 includes an operating system which is stored on media drive 165. Typical operating systems which can be stored on media drive 165 include Microsoft Windows XP, Microsoft Windows 2000 and the Linux operating systems. (Microsoft and Windows are trademarks of Microsoft Corporation.) An expansion bus 170, such as a Peripheral Component Interconnect (PCI) bus, PCI Express bus, SATA bus or other bus is coupled to chipset 125 as shown to enable IHS 100 to be connected to other devices which provide IHS 100 with additional functionality.

Please replace paragraph **[0015]** with the following amended paragraph:

[0015] During the above-described "test window", additional momentary-on logic 230 activates a switch 245 to briefly couple main supply 180 to ground via a test load resistor 250 ~~to ground~~. Thus, power is supplied to test load resistor 250 for a brief instant called the "test period". This test of main supply 180 lasts for just a short test period, for example a 1 sec. test period. Of course the actual duration of the test period can vary. What is important is that for a particular test load resistor power rating the test period be sufficiently long to determine if the power supply is operating properly and sufficiently short in duration that the resistor does not overheat. In this example, the 1 second test period of main supply 180 is within the 10 second test window during which power is supplied to self diagnosis block 210.

Please replace paragraph **[0019]** with the following amended paragraph:

[0019] Once this cool down time delay expires, at block 312, momentary-on logic 220 starts a 10 second "test window" during which diagnostics testing is conducted and completed. Diagnostics block 210 is powered up during the test window and powered down when it ends. The test period includes a short time delay, as per block 315, which is sufficiently long to permit the POWER GOOD output, also called PSU OK, of housekeeping chip 175 to yield a status. Representative time delays are 1mS – 20mS although shorter and longer time delays are acceptable as long as the delay is sufficiently long to yield a POWER GOOD or PSU OK status and sufficiently short to fit within the 10 second test window. Once within the test window and after the above described delay, momentary-on logic 230 briefly closes switch 245 to momentarily supply power from main supply 180 to test load resistor 250 as per block 320. As explained earlier, power is supplied to test load resistor 250 for a short period of time, for example 0.5 to 1 seconds, a period long enough to conduct load testing but not so long that the resistor is overheated. Selecting a very short test period such as above permits the load resistor to be small in both size and expense. Then the PS_ON input of housekeeping chip 175 receives a turn on signal from system board 115 as per block 325. This instructs power supply 105 to turn on. Housekeeping chip 175 generates a POWER GOOD signal, also called PSU OK, which is fed to self diagnostics block 210. The POWER GOOD signal is fed to indicator controller 255 so that controller 255 can be apprised as to how well power supply 105 is functioning.